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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,131	09/19/2001	Tomoaki Yabe	02372.00031	8398

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EXAMINER	
JOSEPH, JAISON	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,131	YABE, TOMOAKI	
	Examiner	Art Unit	
	Jaison Joseph	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1- 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 12-14* is/are rejected.

7)☒ Claim(s) *4-11 and 15-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Volk et al (US Patent 4,680,516).

Regarding claim 1 Volk et al teach phase comparator 109 (see figure 10) having first, second and third flip-flops, and a flip-flop control circuit configured to set the output state of the first flip-flop based on the second and third flip-flops, setting the output state of the second flip-flop based on first and third flip-flops and setting the output state of the third flip-flop based on the outputs of first and second flip-flops, and an up/down signal circuit to output the up signal and the down signal based on the outputs of second and third flip-flops.

Regarding claim 2, Volk et al teach that a flip-flop control circuit brings the first to third flip-flops to set or reset state regardless the what the up and down signal is (see figure 10 component 104a). The up and down control signals do not have feedback to the flip-flop control circuit.

Regarding claim 3, Volk et al teach that the output of the flip-flop 101 is coupled to the reset input of flip-flops 102 and 103 (see column 11 line 58 and 59). Further, the

output of flip-flop 102 and the output of flip-flop 103 are coupled to a NAND gate and the output of the NAND gate is used to reset the flip-flop 101 (see column 11 line 60-64). Therefore, the flip-flop control circuit brings the first flip-flop to a reset state based on the outputs of the second and third flip-flops, brings the second flip-flop to reset state based on the outputs of first and third flip-flops, and brings the third flip-flop to reset state based on the outputs of the first and second flip-flops.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 12, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US patent 5705947) in view of Volk et a (US patent 4,680,516).

Regarding claim 12, Jeong teaches a phase locked loop circuit having a charge pump (see figure 4 components 81 and 82) to output a voltage signal in accordance with an up and down signal, a loop filter (see figure4) to remove the high frequency component included in the output of charge pump, a voltage controlled oscillation circuit (see figure 4) a frequency signal in accordance with the output voltage of the loop filter, a clock buffer (see figure 4 component 90) to output a clock signal in accordance with the output of the voltage controlled oscillator circuit, and a phase detector (see figure 4 component 64) configured to output up and down control signal. Jeong failed to teach a phase detector having first, second, and third flip-flops, a flip-flop control circuit to set

the output state of the first flip-flop based on the output of second and third flip-flop, setting the output second flip-flop based on the output of the first and third flip-flops, and setting the output state of the third flip-flop based on the output of first and second flip-flops, and an up/down signal output circuit to output up signal and down signal based on the outputs of second and third flip-flops. However, Volk et al teach phase comparator 109 (see figure 10) having first, second and third flip-flops, and a flip-flop control circuit configured to set the output state of the first flip-flop based on the second and third flip-flops, setting the output state of the second flip-flop based on first and third flip-flops and setting the output state of the third flip-flop based on the outputs of first and second flip-flops and an up/down signal circuit to output the up signal and the down signal based on the outputs of second and third flip-flops.

Regarding claim 13, which inherits the limitations of claim 12, Jeong teaches that the first signal is a reference signal supplied from the outside (see figure 4 signal 70) and the second clock signal is a signal correlated with the clock signal outputted from the clock buffer (see figure 4 signal 80).

Regarding claim 14, which inherits the limitations of claim 12, Volk et al teach that the output of the flip-flop 101 is coupled to the reset input of flip-flops 102 and 103 (see column 11 line 58 and 59). Further, the output of flip-flop 102 and the output of flip-flop 103 are coupled to a NAND gate and the output of the NAND gate is used to reset the flip-flop 101 (see column 11 line 60-64). Therefore, the flip-flop control circuit brings the first flip-flop to a reset state based on the outputs of the second and third flip-flops, brings the second flip-flop to reset state based on the outputs of first and third flip-flops,

and brings the third flip-flop to reset state based on the outputs of the first and second flip-flops.

Allowable Subject Matter

Claims 4-11 and 15-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jaison Joseph whose telephone number is (571) 272-6041. The examiner can normally be reached on M-F 8:30 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jaison Joseph
Patent Examiner

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